WHAT IS CLAIMED IS:

1. A hysteretic amplifier comprising:

a first differential pair of first and second transistors receiving first and second input voltages and generating and a first output voltage;

third and fourth transistors coupled to the first and second transistors, respectively, and coupled to receive first and second control signals, respectively; and

a multiplexer that generates the first and the second control signals in response a hysteretic select signal,

wherein the multiplexer causes the hysteretic amplifier to have positive hysteresis when the hysteretic select signal is in a first state, and the multiplexer causes the hysteretic amplifier to have negative hysteresis when the hysteretic select signal is in a second state.

2. The hysteretic amplifier as defined in claim 1 wherein the multiplexer causes the hysteretic amplifier to not have hysteretic input thresholds when a disable signal is in a first state.

3. The hysteretic amplifier as defined in claim 1 further comprising:

fifth and sixth transistors coupled in parallel to the third and fourth transistors, respectively, and coupled to receive third and fourth control signals, respectively,

wherein the first, the second, the third, and the fourth control signals are generated by the multiplexer in response to the hysteretic select signal and a plurality of program signals.

4. The hysteretic amplifier as defined in claim 1 further comprising:

fifth and sixth transistors coupled to the third and fourth transistors, respectively, and coupled to receive the first and second input voltages.

5. The hysteretic amplifier as defined in claim 1 wherein the hysteretic amplifier is an input buffer coupled to receive input signals from an input pin of an integrated circuit.

6. The hysteretic amplifier as defined in claim 5 wherein the integrated circuit is a field programmable gate array.

7. The hysteretic amplifier as defined in claim 1 further comprising:

a first resistor coupled to a drain of the first transistor;

a second resistor coupled to a drain of the second transistor;

a third resistor coupled to a drain of the third transistor; and

a fourth resistor coupled to a drain of the fourth transistor.

8. The hysteretic amplifier as defined in claim 1 further comprising:

a second differential pair of fifth and sixth transistors receiving the first and the second input voltages and generating and a second output voltage; and

seventh and eighth transistors coupled to the fifth and sixth transistors, respectively, and coupled to receive the first and the second control signals, respectively.

9. The hysteretic amplifier as defined in claim 8 wherein the hysteretic amplifier is a two stage hysteretic amplifier that further comprises an output stage, the output stage comprising:

a third different pair of ninth and tenth transistors coupled to receive the first output voltage of the first differential pair and the second output voltage of the second differential pair; and

eleventh and twelfth transistors coupled to the ninth and tenth transistors, respectively, and coupled to receive third and fourth control signals, respectively,

wherein the third and the fourth control signals control hysteretic threshold levels of the output stage.

10. A method for amplifying an input signal, the method comprising:

amplifying a difference between first and second input signals to generate an output signal;

causing the output signal to change state at first and second hysteretic thresholds when a hysteretic select signal is in a first state, the first and second hysteretic thresholds occurring after the first and second input signals cross a common point; and

causing the output signal to change state at third and fourth hysteretic thresholds when the hysteretic select signal is in a second state, the third and fourth hysteretic thresholds occurring before the third and fourth input signals cross the common point.

11. The method according to claim 10 further comprising:

causing the output signal to change state at a fifth non-hysteretic threshold level when a disable signal is in a first state.

12. The method according to claim 10 wherein the first, the second, the third, and the fourth hysteretic threshold levels are adjustable by changing logic states of a plurality of program signals.

13. The method according to claim 10 wherein amplifying the difference between the first and the second input signals to generate the output signal further comprises:

amplifying the difference between the first and the second input signals using a first differential pair of transistors to generate a first pre-amplified signal;

amplifying the difference between first and the second input signals using a second differential pair of transistors to generate a second pre-amplified signal; and

amplifying a difference between the first and the second pre-amplified signals using a third differential pair of transistors to generate the output signal.

14. The method according to claim 10 further comprising:

selecting the output signal as a first control signal and selecting an inversion of the output signal as a second control signal when the hysteretic select signal is in a first state; and

selecting the inversion of the output signal as the first control signal and selecting the output signal as the second control signal when the hysteretic select signal is in a second state.

15. The method according to claim 14 wherein the output signal changes state in response to the first and the second control signals.

16. A hysteretic amplifier comprising:

means for amplifying a difference between first and second input signals to generate and an output signal;

means for generating first and second control signals in response a hysteretic select signal and the output signal,

means for switching a level of the output signal at first and second positive hysteretic thresholds when a hysteretic select signal is in a first state; and

means for switching the level of the output signal at third and fourth negative hysteretic thresholds when the hysteretic select signal is in a second state.

17. The hysteretic amplifier according to claim 16 further comprising:

means for switching the level of the output signal at a fifth non-hysteretic threshold when a disable signal is in a first state.

18. The hysteretic amplifier according to claim 16 further comprising:

means for switching the level of the output signal at a fifth positive hysteretic threshold when the hysteretic select signal is in the first state and a first program signal is in a first state; and

means for switching the level of the output signal at a sixth negative hysteretic threshold when the hysteretic select signal is in the second state and a second program signal is in a first state.

19. The hysteretic amplifier according to claim 16 wherein the hysteretic amplifier is an input buffer coupled to receive input signals from an input pin of an integrated circuit.

20. A two stage amplifying system comprising

first and second hysteretic amplifiers coupled to receive first and second differential input voltages; and

a third hysteretic amplifier having inputs coupled to outputs of the first and the second amplifiers,

wherein the first and the second hysteretic amplifiers generate two positive hysteretic thresholds in response to first and second control signals, and two negative hysteretic thresholds in response to the first and the second control signals,

and the third hysteretic amplifier generates two positive hysteretic thresholds in response to third and fourth control signals, and two negative hysteretic thresholds in response to the third and the fourth control signals.